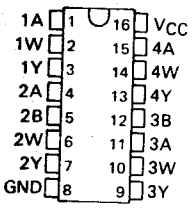
REVISED DECEMBER 1983

FOR SYMMETRICAL GENERATION OF COMPLEMENTARY TTL SIGNALS

- Switching Time Skew of the Complementary Outputs Is Typically 0.5 ns . . . Guaranteed to be No More than 3 ns at Rated Loading
- Full Fan-Out to 20 High-Level and 10 Low-Level 54/74 Loads
- Active Pull-Down Provides Square Transfer Characteristic

SN54265 . . . J OR W PACKAGE
SN74265 . . . J OR N PACKAGE
(TOP VIEW)



NC - No internal connection

description

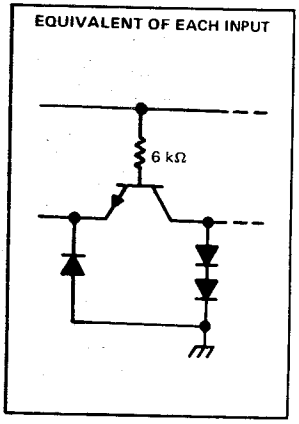
The SN54265 and SN74265 circuits feature complementary outputs from each logic element, which have virtually symmetrical switching time delays from the triggering input. They are designed specifically for use in applications such as:

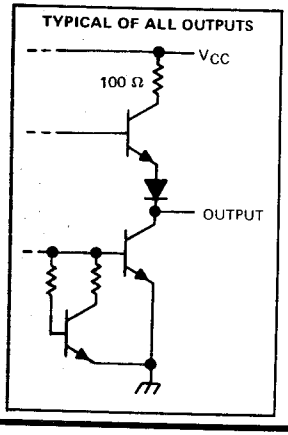
- Symmetrical clock/$\overline{\text{clock}}$ generators
- Complementary input circuit for decoders and code converters
- Switch debouncing
- Differential line driver

Examples of these four functions are illustrated in the typical application data.

The SN54265 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74265 is characterized for operation from 0°C to 70°C.

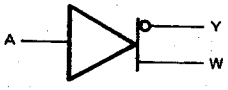
schematics of inputs and outputs





logic diagrams

ELEMENTS 1 and 4



positive logic

$Y = \overline{A}$ $\quad W = A$

ELEMENTS 2 and 3

positive logic

$Y = \overline{AB}$ or $Y = \overline{A} + \overline{B}$
$W = AB$ or $W = \overline{\overline{A} + \overline{B}}$

TEXAS INSTRUMENTS
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